IN THE CLAIMS:

Please amend claims 151, 159, 169, 177, 182, 184, 185, 187, and 188 as indicated below.

A listing of the status of all claims 1-188 in the present patent application is provided below.

1-150 (Cancelled).

151 (Currently Amended). A method of operating a controller device, comprising:

outputting a value to a memory device;

outputting a first operation code to the memory device, wherein the first operation code instructs the memory device to store the value in a register of the memory device;

outputting a block size value to the memory device, wherein the block size value indicates an amount of read data to be output by the memory device in response to a second operation code;

outputting the second operation code to the memory device, wherein the second operation code instructs the memory device to perform a read operation, wherein the second operation code includes precharge information that indicates whether the memory device should precharge sense amplifiers on the memory device

after sensing data corresponding to the read operation; and

after a read delay following the outputting of the second operation code, sampling a first portion of the read data output by the memory device in response to the second operation code, wherein the read delay is selected to correspond to ~~determined using~~ the value output to the memory device for storage in the register.

152 (Previously Presented). The method of claim 151, wherein outputting the first and second operation codes further comprises outputting the first and second operation codes synchronously with respect to a clock signal.

153 (Previously Presented). The method of claim 151, wherein outputting the first operation code further comprises outputting the first operation code using pads on the controller device, the pads to connect to a set of external signal lines, and wherein outputting the second operation code further comprises outputting the second operation code using the pads on the controller device used to output the first operation code.

154 (Previously Presented). The method of claim 151, wherein sampling the first portion of the read data further comprises:

for a pad on the controller device from which read data is sampled, sampling two bits of read data from the pad during a clock cycle of a clock signal used by the controller device.

155 (Previously Presented). The method of claim 154, wherein sampling the first portion of the read data further comprises:

for each pad on the controller device from which read data is sampled, sampling two bits of read data during a clock cycle of a clock signal used by the controller device.

156 (Previously Presented). The method of claim 154, further comprising generating the clock signal internal to the controller device.

157 (Previously Presented). The method of claim 156, wherein generating the clock signal further comprises:

receiving first and second external clock signals; and

generating the clock signal using the first and second external clock signals.

158 (Previously Presented). The method of claim 154, further comprising receiving the clock signal from external to the controller device.

159 (Currently Amended). The method of claim 154, further comprising:

outputting a third operation code to the memory device, wherein the third operation code instructs the memory device to perform a write operation; and

after a write delay following the outputting of the third operation code, outputting write data to the memory device, wherein the write delay is selected to correspond to ~~determined using~~ the value output to the memory device for storage in the register.

160 (Previously Presented). The method of claim 159, wherein the write data is output synchronously with respect to the clock signal.

161 (Previously Presented). The method of claim 160, wherein the second operation code is output synchronously with respect to the clock signal.

162 (Previously Presented). The method of claim 161, further comprising:

outputting first address information to the memory device,

wherein the first address information indicates a location in a memory array of the memory device at which the read data is stored; and

outputting second address information to the memory device, wherein the second address information indicates a location in the memory array at which the write data is to be stored.

163 (Previously Presented). The method of claim 162, wherein outputting the write data to the memory device further comprises, for a pad on the controller device used to output write data, outputting two bits of write data using the pad during a clock cycle of the clock signal.

164 (Previously Presented). The method of claim 163, wherein outputting the write data to the memory device further comprises, for each pad on the controller device used to output write data, outputting two bits of write data during a clock cycle of the clock signal.

165 (Previously Presented). The method of claim 163, wherein outputting the value further comprises outputting the value to the memory device via an external bus, wherein the first address information and the second address information are also output

to the memory device via the external bus.

166 (Previously Presented). The method of claim 165, wherein the read delay and the write delay are about the same.

167 (Previously Presented). The method of claim 166, wherein outputting the block size value and outputting the second operation code further comprises outputting the block size value and the second operation code to the memory device in a packet.

168 (Previously Presented). The method of claim 151, further comprising sampling the amount of read data output by the memory device in response to the second operation code, wherein the amount of read data is sampled over a plurality of clock cycles of a clock signal used by the controller device to output the first and second operation codes, and wherein sampling the amount of read data includes sampling the first portion of the read data.

169 (Currently Amended). A controller device, comprising:

output driver circuitry, the output driver circuitry to:

output a value to a memory device;

output a first operation code to the memory device,

wherein the first operation code instructs the memory device to store the value in a register in the memory device;

output a block size value to the memory device, wherein the block size value indicates an amount of read data to be output by the memory device in response to a second operation code; and

output the second operation code to the memory device, wherein the second operation code instructs the memory device to perform a read operation, wherein the second operation code includes precharge information that indicates to the memory device whether the memory device should precharge sense amplifiers on the memory device after sensing data corresponding to the read operation; and

input receiver circuitry to sample a first portion of the read data output by the memory device in response to the second operation code, the input receiver circuitry to sample the first portion of the read data after a read delay following the outputting of the second operation code, wherein the read delay is selected to correspond to ~~determined using~~ the value output to the memory device for storage in the register.

170 (Previously Presented). The controller device of claim 169, further comprising a plurality of pads to interface with

signal lines external to the controller device, wherein the input receiver circuitry is coupled to a first portion of the plurality of pads to receive the first portion of the read data, and wherein for a pad used in the receipt of the first portion of the read data, two bits of read data are received from the pad during a clock cycle of a clock signal used by the controller device.

171 (Previously Presented). The controller device of claim 170, wherein for each pad used in the receipt of the first portion of the read data, two bits of read data are received during a clock cycle of the clock signal.

172 (Previously Presented). The controller device of claim 170, further comprising a clock receiver to receive the clock signal from external to the controller device.

173 (Previously Presented). The controller device of claim 170, further comprising a clock generation circuit to generate the clock signal.

174 (Previously Presented). The controller device of claim 173, further comprising:

a first clock receiver to receive a first external clock signal; and

a second clock receiver to receive a second external clock signal,

wherein the clock generation circuit is coupled to the first and second clock receivers, and wherein the clock generation circuit generates the clock signal using the first and second external clock signals.

175 (Previously Presented). The controller device of claim 170, wherein the input receiver circuitry includes, for each pad of the plurality of pads used to receive read data, a first input receiver and a second input receiver.

176 (Previously Presented). The controller device of claim 169, wherein the output driver circuitry outputs a third operation code to the memory device, wherein the third operation code instructs the memory device to perform a write operation.

177 (Currently Amended). The controller device of claim 176, wherein the output driver circuitry outputs write data to the memory device after a write delay following outputting of the third operation code, wherein the write delay is selected to

correspond to ~~determined using~~ the value output to the memory device for storage in the register.

178 (Previously Presented). The controller device of claim 177, wherein the output driver circuitry includes a plurality of output drivers, wherein the output driver circuitry outputs at least a portion of the write data using output drivers of the plurality of output drivers that are also used to output the first operation code to the memory device.

179 (Previously Presented). The controller device of claim 177, wherein the output driver circuitry includes a plurality of output drivers, wherein an output driver of the plurality of output drivers outputs two bits of the write data during a clock cycle of a clock signal used by the controller device.

180 (Previously Presented). The controller device of claim 179, further comprising a clock receiver to receive the clock signal, wherein the output driver circuitry outputs the write data synchronously with respect to the clock signal.

181 (Previously Presented). The controller device of claim 169, wherein the output driver circuitry includes:

a first set of output drivers to output the first operation code; and

a second set of output drivers to output the block size value.

182 (Currently Amended). A method of controlling a memory device by a controller device, comprising:

outputting a value to the memory device;

outputting a first operation code to the memory device, wherein the first operation code instructs the memory device to store the value in a register of the memory device;

outputting a second operation code to the memory device, wherein the second operation code instructs the memory device to perform a read operation, wherein the second operation code includes precharge information that indicates whether the memory device should precharge sense amplifiers on the memory device after sensing data corresponding to the read operation; and

after a read delay following the outputting of the second operation code, sampling a first portion of read data output by the memory device in response to the second operation code, wherein the read delay is selected to correspond to ~~determined using~~ the value output to the memory device for storage in the register.

183 (Previously Presented). The method of claim 182, wherein sampling the first portion of read data further comprises:

for each pad on the controller device from which read data is sampled, sampling two bits of read data during a clock cycle of a clock signal used by the controller device.

184 (Currently Amended). The method of claim 183, further comprising:

outputting a third operation code to the memory device, wherein the third operation code instructs the memory device to perform a write operation; and

after a write delay following the outputting of the third operation code, outputting write data to the memory device, wherein the write delay is selected to correspond to ~~determined using~~ the value output to the memory device for storage in the register, wherein outputting the write data to the memory device further comprises, for each pad on the controller device used to output write data, outputting two bits of write data during a clock cycle of the clock signal.

185 (Currently Amended). A controller device, comprising:

means for outputting a value to ~~the~~ a memory device;

means for outputting a first operation code to the memory device, wherein the first operation code instructs the memory device to store the value in a register of the memory device;

means for outputting a block size value to the memory device, wherein the block size value indicates an amount of read data to be output by the memory device in response to a second operation code;

means for outputting the second operation code to the memory device, wherein the second operation code instructs the memory device to perform a read operation, wherein the second operation code includes precharge information that indicates whether the memory device should precharge sense amplifiers on the memory device after sensing data corresponding to the read operation; and

means for sampling read data, wherein after a read delay following the outputting of the second operation code, the means for sampling read data samples a first portion of the read data output by the memory device in response to the second operation code, wherein the read delay is selected to correspond to ~~determined using~~ the value output to the memory device for storage in the register.

186 (Previously Presented). The controller device of claim

185, further comprising:

for each pad on the controller device from which read data is sampled, means for sampling two bits of read data during a clock cycle of a clock signal used by the controller device.

187 (Currently Amended). The controller device of claim 186, further comprising:

means for outputting a third operation code to the memory device, wherein the third operation code instructs the memory device to perform a write operation; and

means for outputting write data to the memory device, wherein after a write delay following the outputting of the third operation code, the means for outputting write data to the memory device outputs write data to the memory device, wherein the write delay is selected to correspond to ~~determined using~~ the value output to the memory device for storage in the register, wherein outputting the write data to the memory device further comprises, for each pad on the controller device used to output write data, outputting two bits of write data during a clock cycle of the clock signal.

188 (Currently Amended). A controller device, comprising:

output driver circuitry, the output driver circuitry to:

output a value;

output a first operation code, wherein the first operation code represents an instruction to a memory device to store the value in a register in the memory device;

output a block size value, wherein the block size value indicates an amount of read data to be output by the memory device in response to a second operation code; and

output the second operation code, wherein the second operation code represents an instruction to the memory device to perform a read operation, wherein the second operation code includes an indication to the memory device as to whether the memory device should precharge sense amplifiers on the memory device after sensing data corresponding to the read operation; and

input receiver circuitry to sample a first portion of the read data output by the memory device, the input receiver circuitry to sample the first portion of the read data after a read delay following the outputting of the second operation code, wherein the read delay is selected to correspond to ~~determined using~~ the value.